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Implementation of high-side, high-voltage RESUR LDMOS in a sub-half micron smart power technol

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Abstract:
55 V high-side RESURF LDMOS has been integrated successfully in 0.35 μm smart power technology by carefully arranging the lateral doping profile. This device has Rds.on×area of 0.55 mΩ.cm ^{2} with excellent safe operating With proper device terminal biasing scheme, this device can also be used as an isolated device. Techniques and issues related to the isolation is considered an discussed

Index Terms:
doping profiles isolation technology power MOSFET power integrated circuits 0.35 mi 55 V device isolation high-side high-voltage RESURF LDMOS transistor lateral doping profile safe operating area smart power technology terminal biasing

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